ECVEM
European Centre of Vocational Excellence in Microelectronics

WP3 Course development, learning environment and course format, examples by partners (UNED, all)

UNED (P16)

UNED

Co-funded by the Erasmus+ Programme of the European Union

WP3: Cases and course drafts

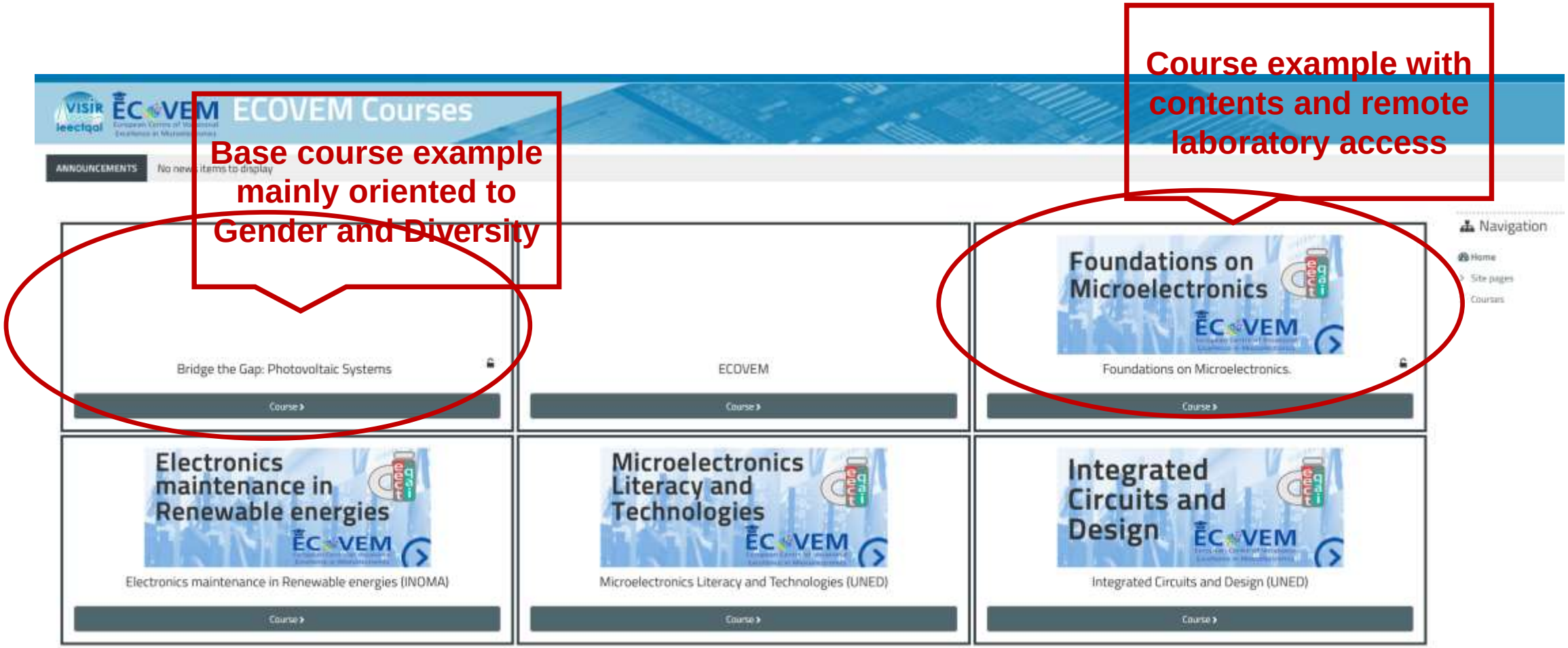
Moodle UNED courses examples access

http://62.204.201.34/moodle/?lang=en

Form questionnaire getting information

https://forms.gle/dxk2cnXe7kFgEziT6

WP3: Cases and course drafts



About UNED

Founding in 1972

The largest university in Spain

More than 260,000 students

26 Bachelor's degrees

43 master's degrees

More than 600 Continuing Education programs

12 language courses

More than a hundred Summer Courses

Almost 400 University Extension activities

More than 10,000 people, from the headquarters and from the associated centers

WP3: Design and Development of Innovative VET

Curricula	→	Modular and interdisciplinary
Adapted	→	Blended learning models (educational, job-related projects, lifelong learning)
Scope	→	iVET, cVET, lifelong learning, training, re-training and up-training
Approach	→	relevant skills for labour market
Aligned	→	ESCO, EQF, EQVET and NQFs
Level	→	EQF 3 to 8 levels providing practice of school students in the university laboratories and preparing VET students for technical competitions

Courses

At least half of the courses will be for on-line delivery.

Courses will be provided as open educational resources.

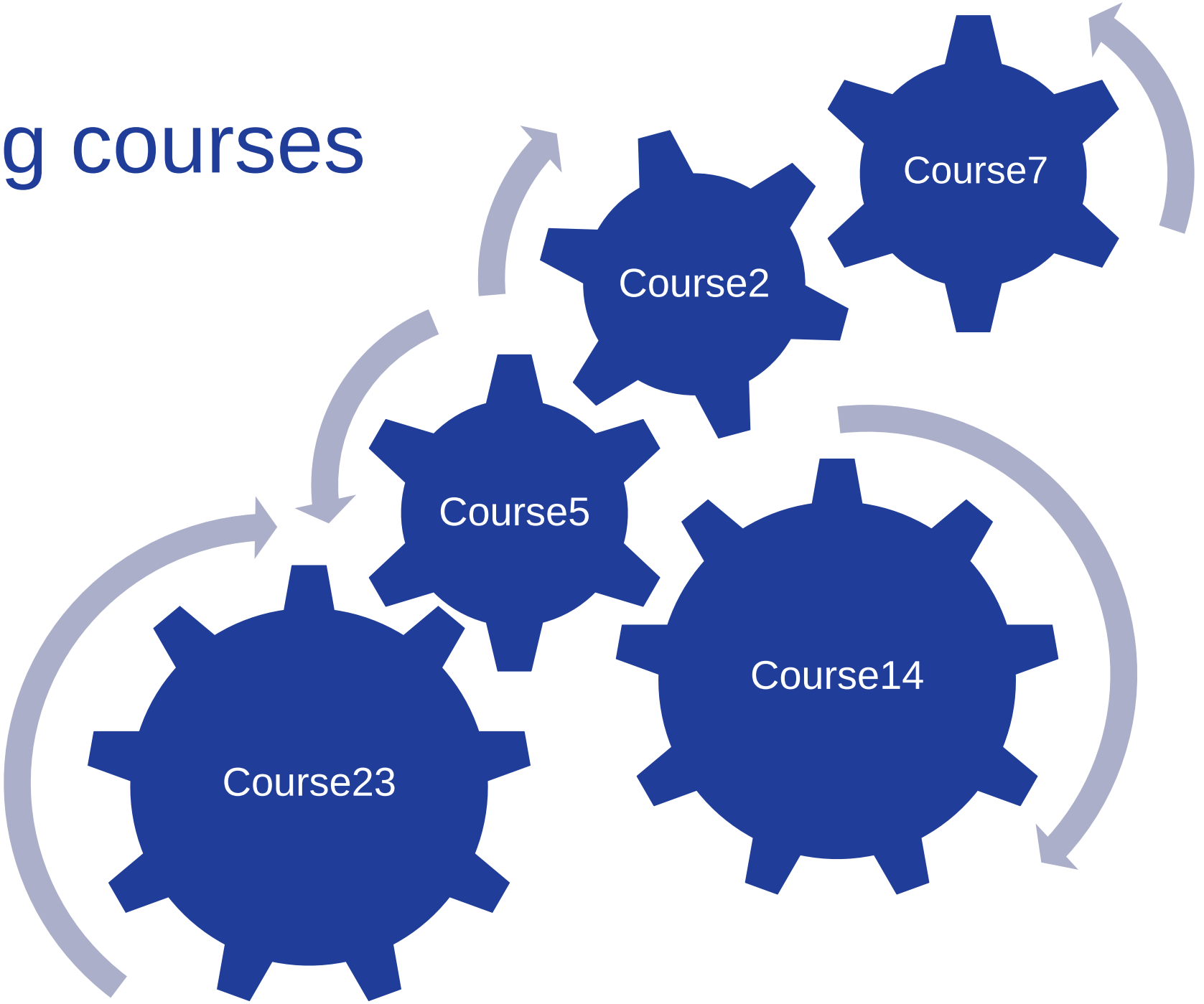
Courses will be delivered in a common cloud-based and rich repository of learning modules.

This mode of delivery of VET will facilitate the virtual mobility in VET.

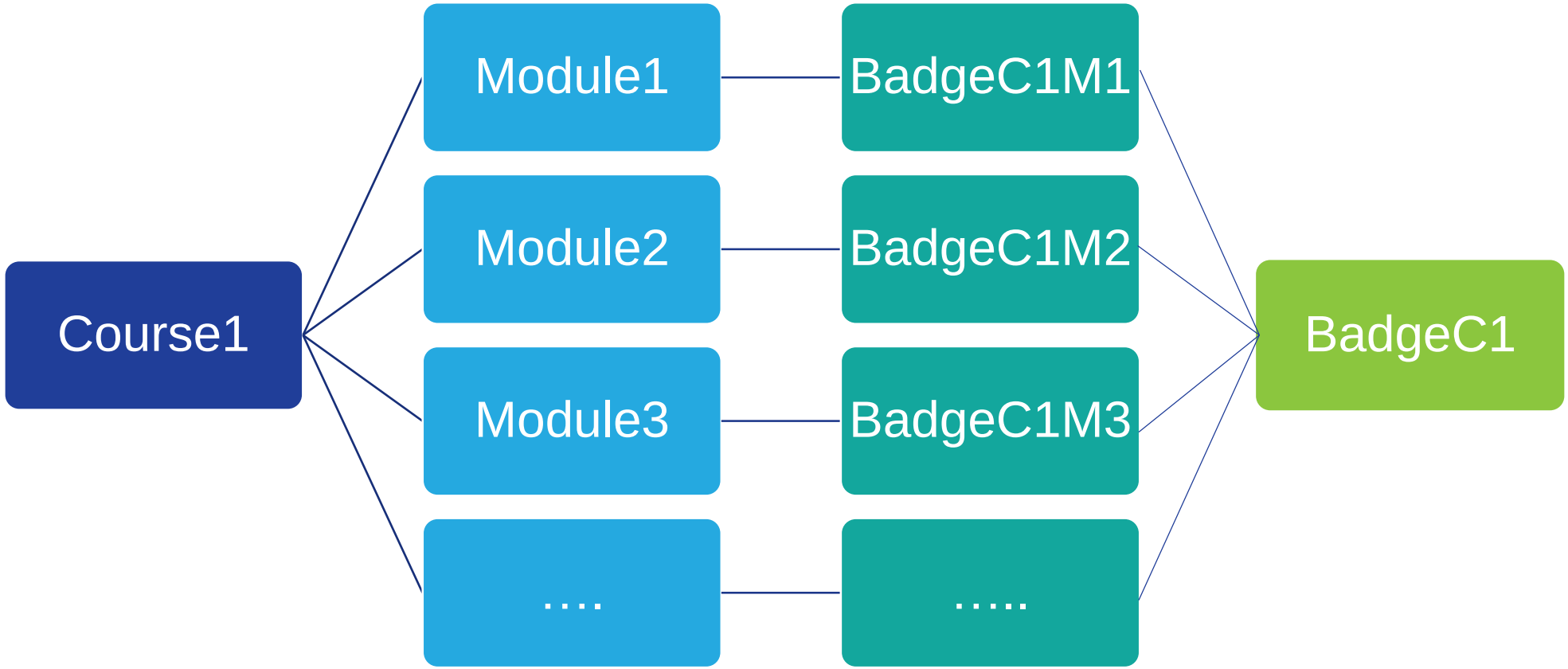
Each course will be designed for specific learning outcomes defined as a result of the educational need and job analysis

50 ECTs --→70-80 ECTs

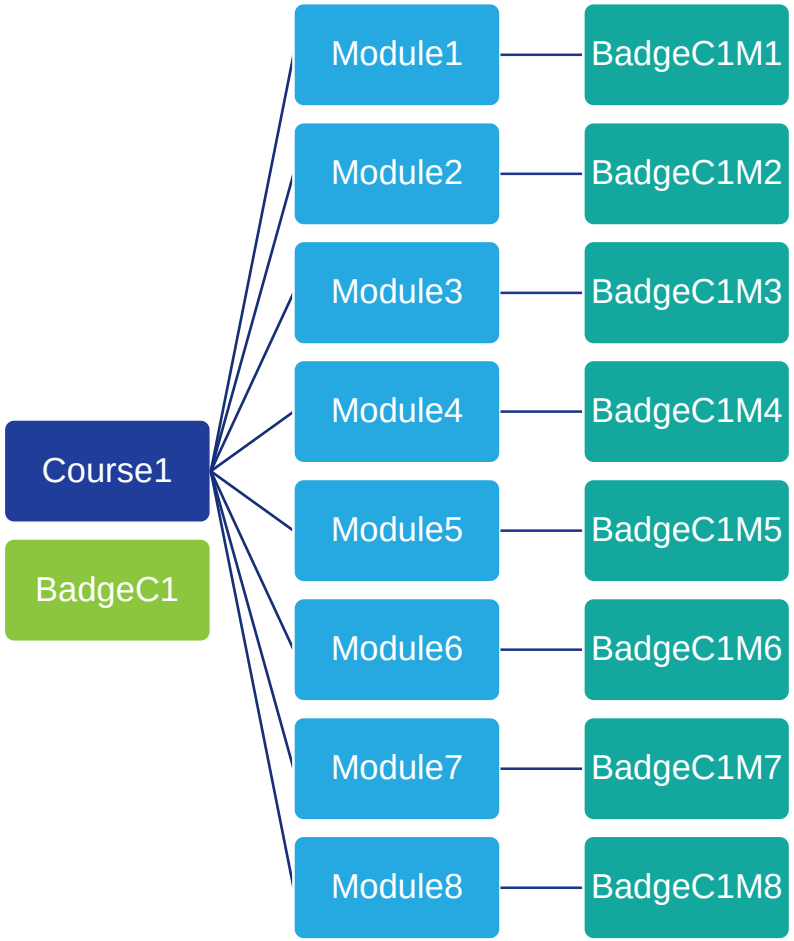
Scaffolding courses

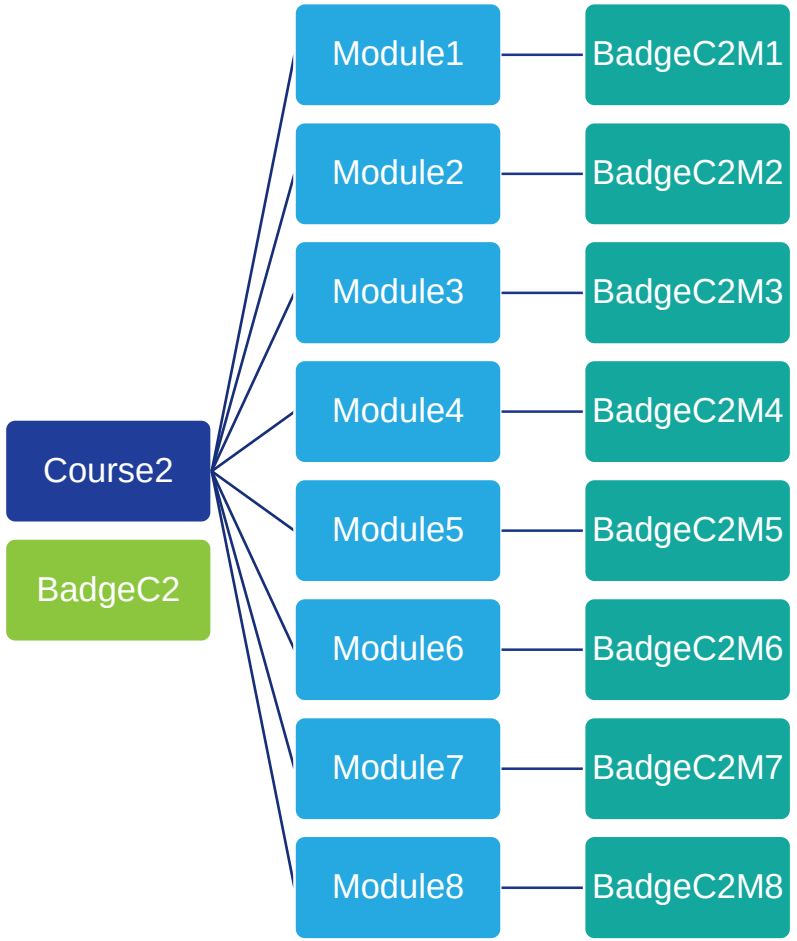


Course design

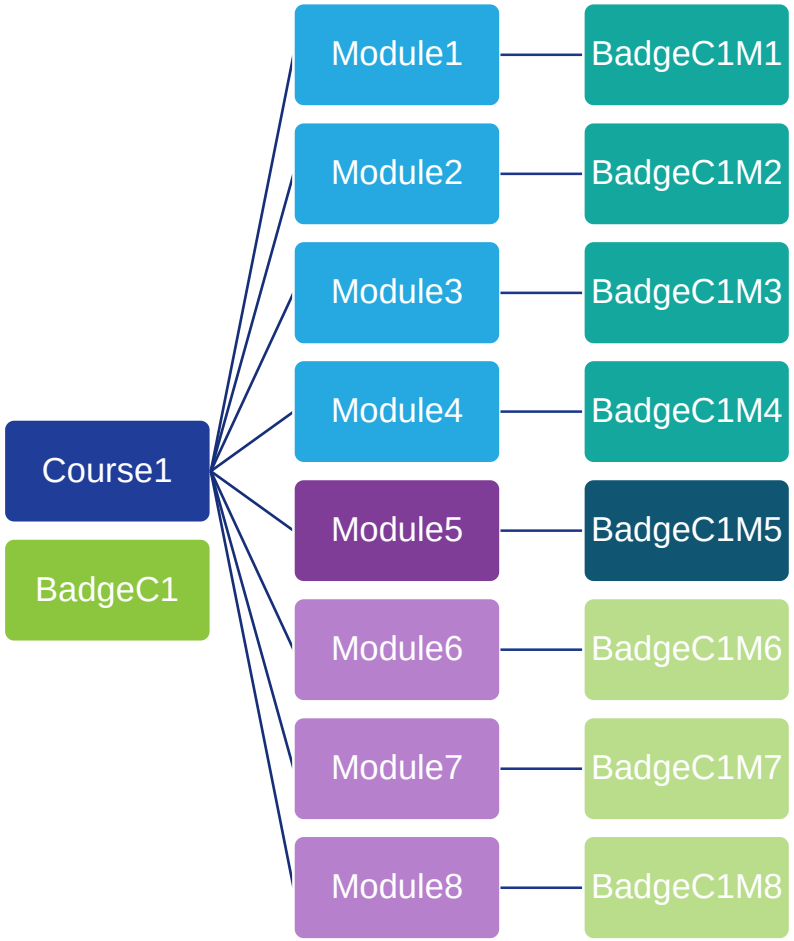


Course design





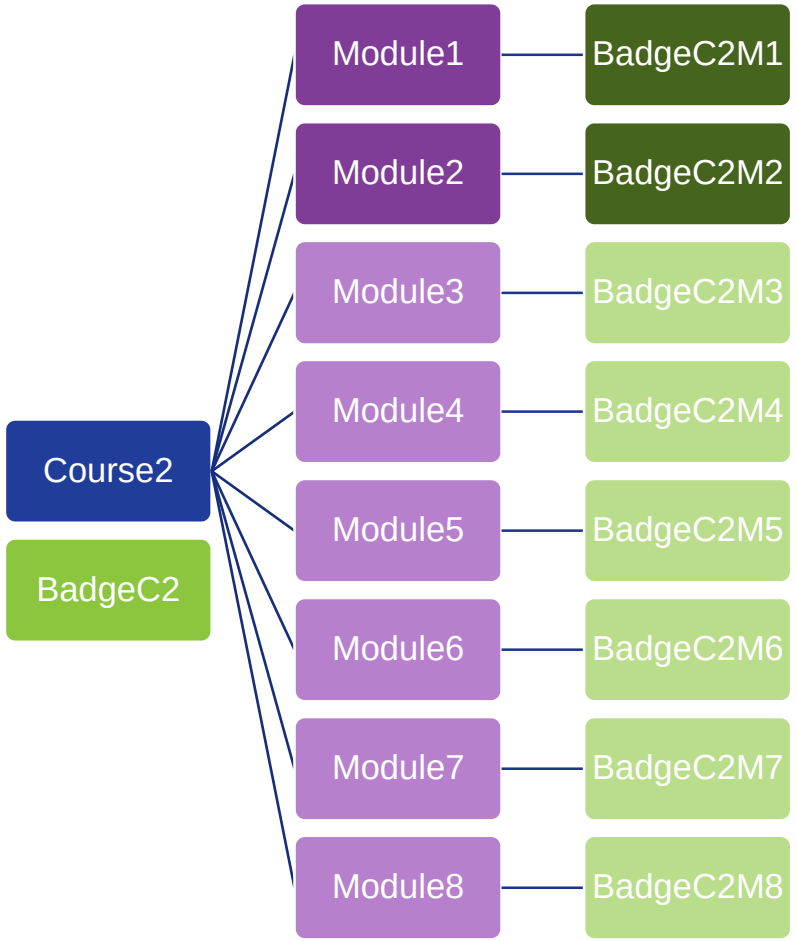
Duplicity



Course1
Module 5 deals with the handling of a simulator named MicroLab

Module 6/7/8 use MicroLab for learning activities.

Course2
MicroLab simulator is integrated in all activities Module 3-8.
Module 1 & 2 are focussed on the handling of MicroLab simulator



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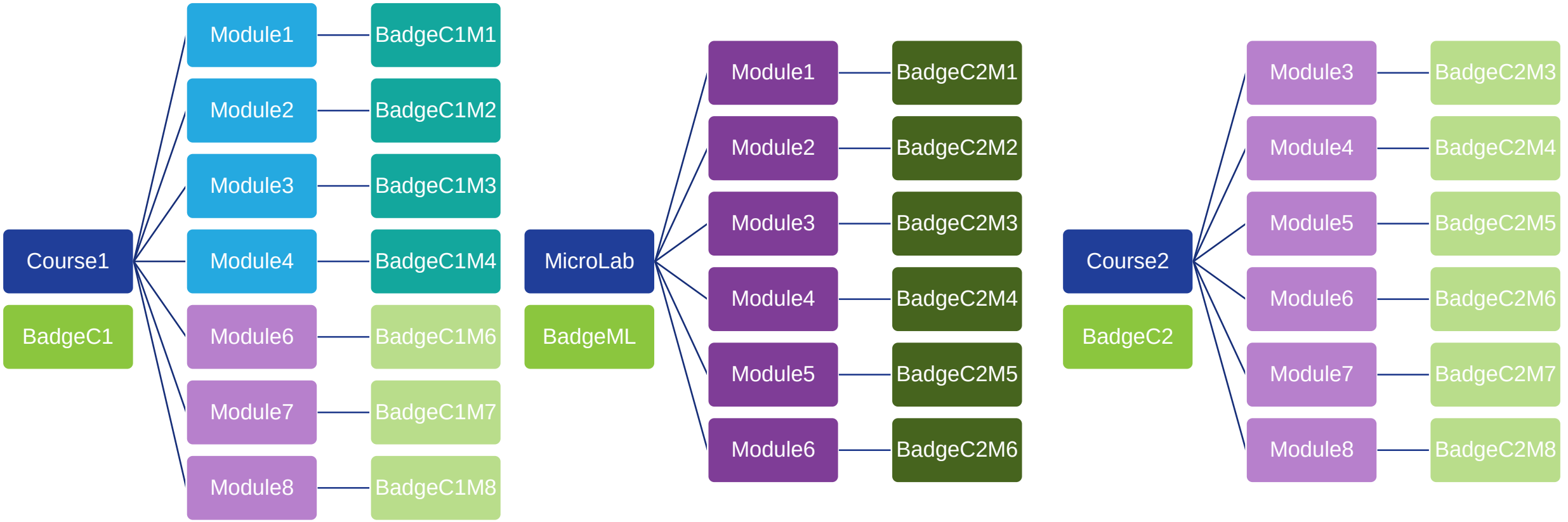
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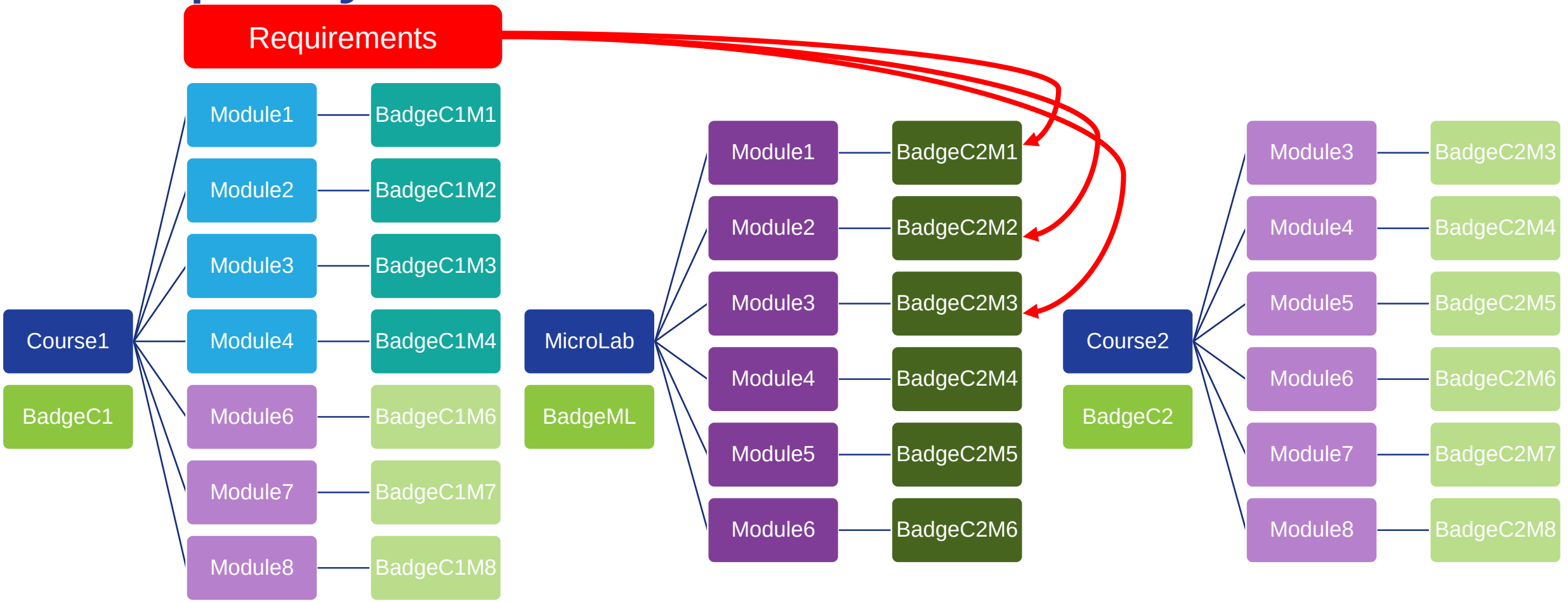
BadgeC1
Module1
Module2
Module3
Module4
Module6
Module7
Module8
BadgeC1M1
BadgeC1M2
BadgeC1M3
BadgeC1M4
BadgeC1M6
BadgeC1M7
BadgeC1M8
MicroLab
BadgeML
Module1
Module2
Module3
Module4
Module5
Module6
BadgeC2M1
BadgeC2M2
BadgeC2M3
BadgeC2M4
BadgeC2M5
BadgeC2M6
Course2
BadgeC2
Module3
Module4
Module5
Module6
Module7
Module8
BadgeC2M3
BadgeC2M4
BadgeC2M5
BadgeC2M6
BadgeC2M7
BadgeC2M8

Duplicity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Module1
Module2
Module3
Module4
Module6
Module7
Module8
BadgeC1M1
BadgeC1M2
BadgeC1M3
BadgeC1M4
BadgeC1M6
BadgeC1M7
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MicroLab
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Course2
BadgeC2
Module3
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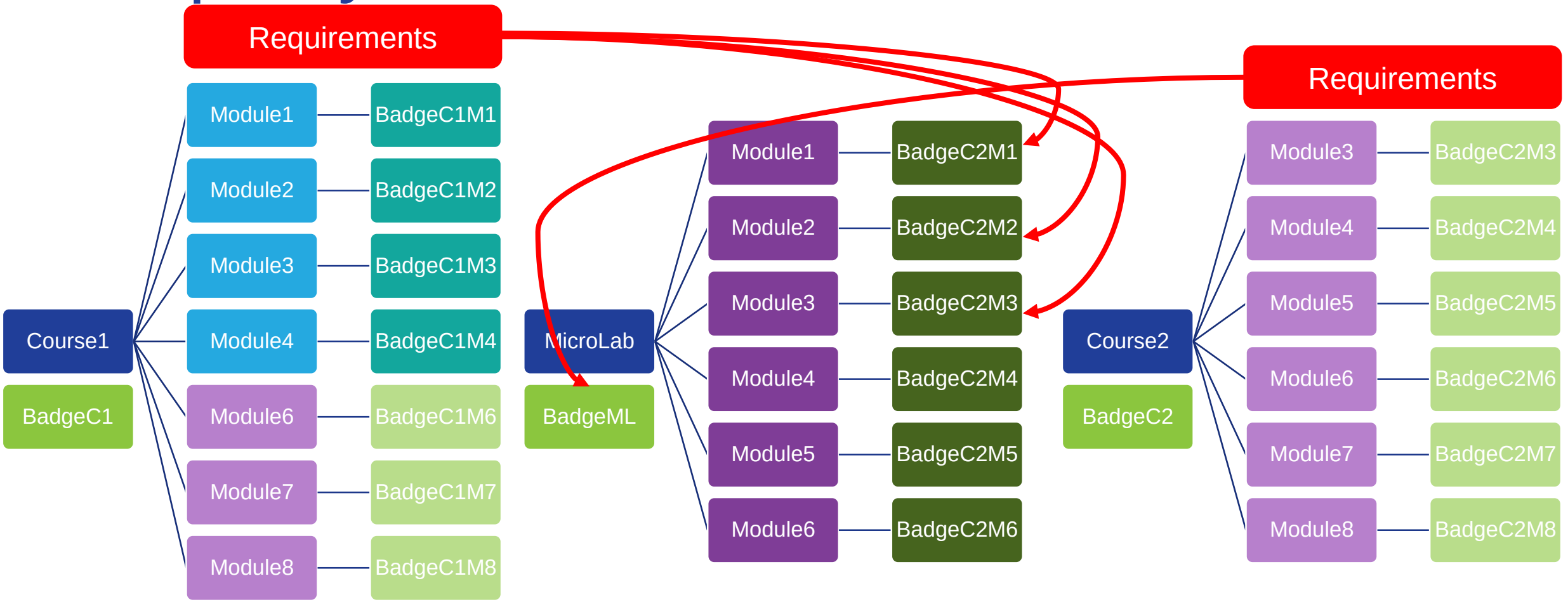
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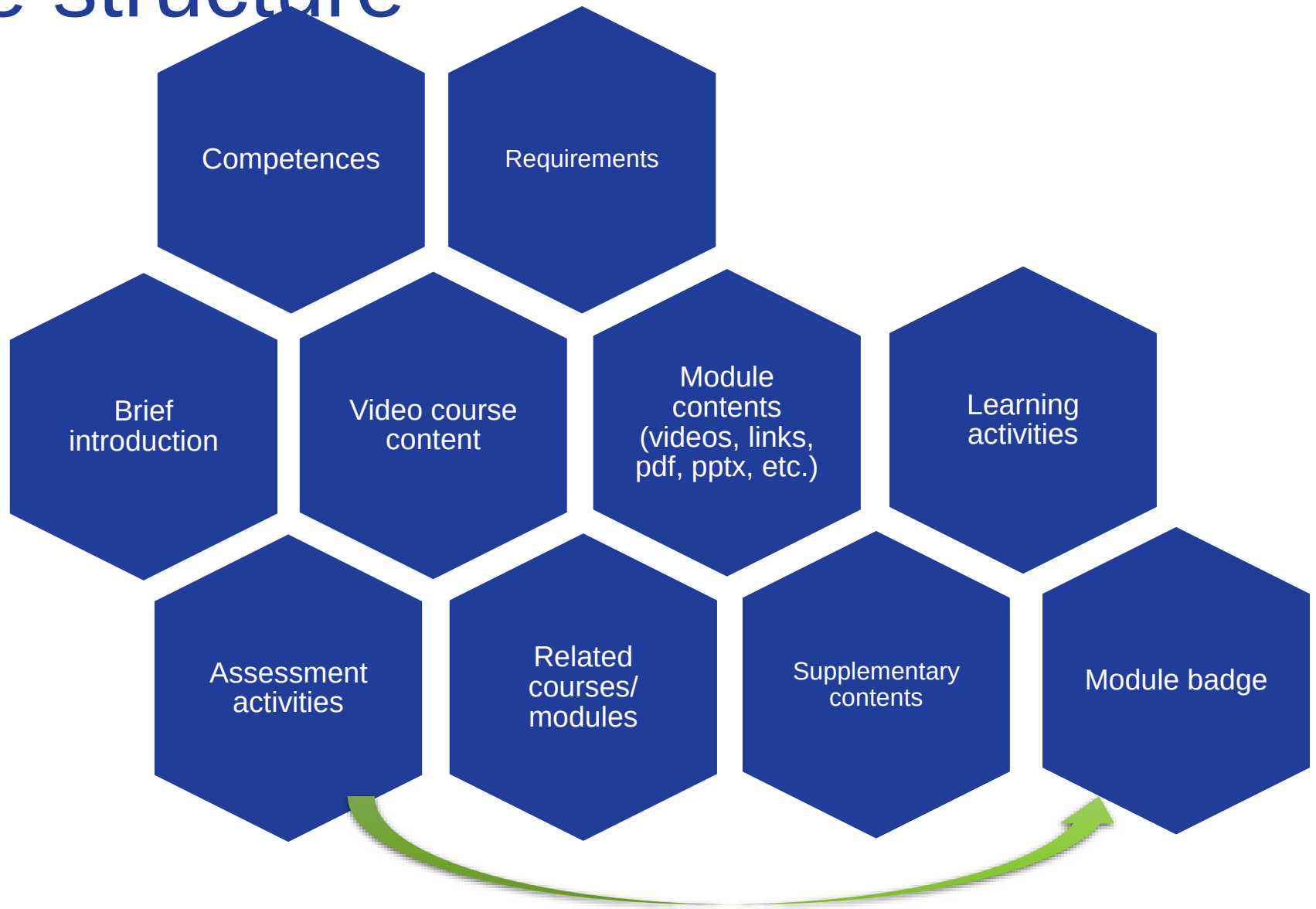
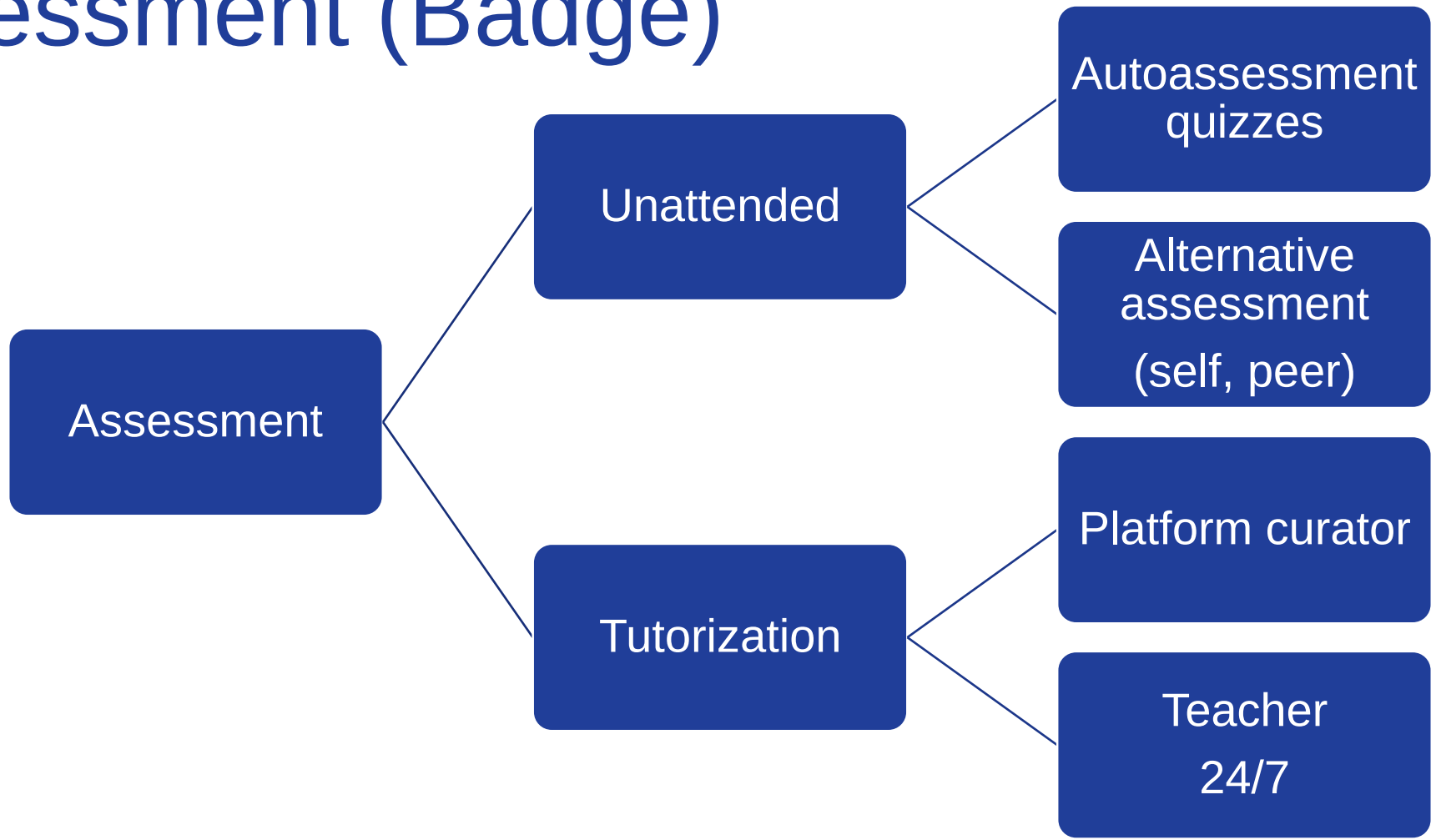
Course1
Module4
BadgeC1M4
BadgeC1
Module6
BadgeC1M6
Module7
BadgeC1M7
Module8
BadgeC1M8
MicroLab
BadgeML
Module1
BadgeC2M1
Module2
BadgeC2M2
Module3
BadgeC2M3
Module4
BadgeC2M4
Module5
BadgeC2M5
Module6
BadgeC2M6
Requirements
Course2
BadgeC2
Module3
BadgeC2M3
Module4
BadgeC2M4
Module5
BadgeC2M5
Module6
BadgeC2M6
Module7
BadgeC2M7
Module8
BadgeC2M8

Module structure



Assessment (Badge)



Practical scenarios

		Experimenter location	
		LOCAL	REMOTE
Experiment nature	REAL	HANDS-ON LAB	REMOTE LAB
	SIMULATED	SIMULATOR	VIRTUAL LAB

Lab practices

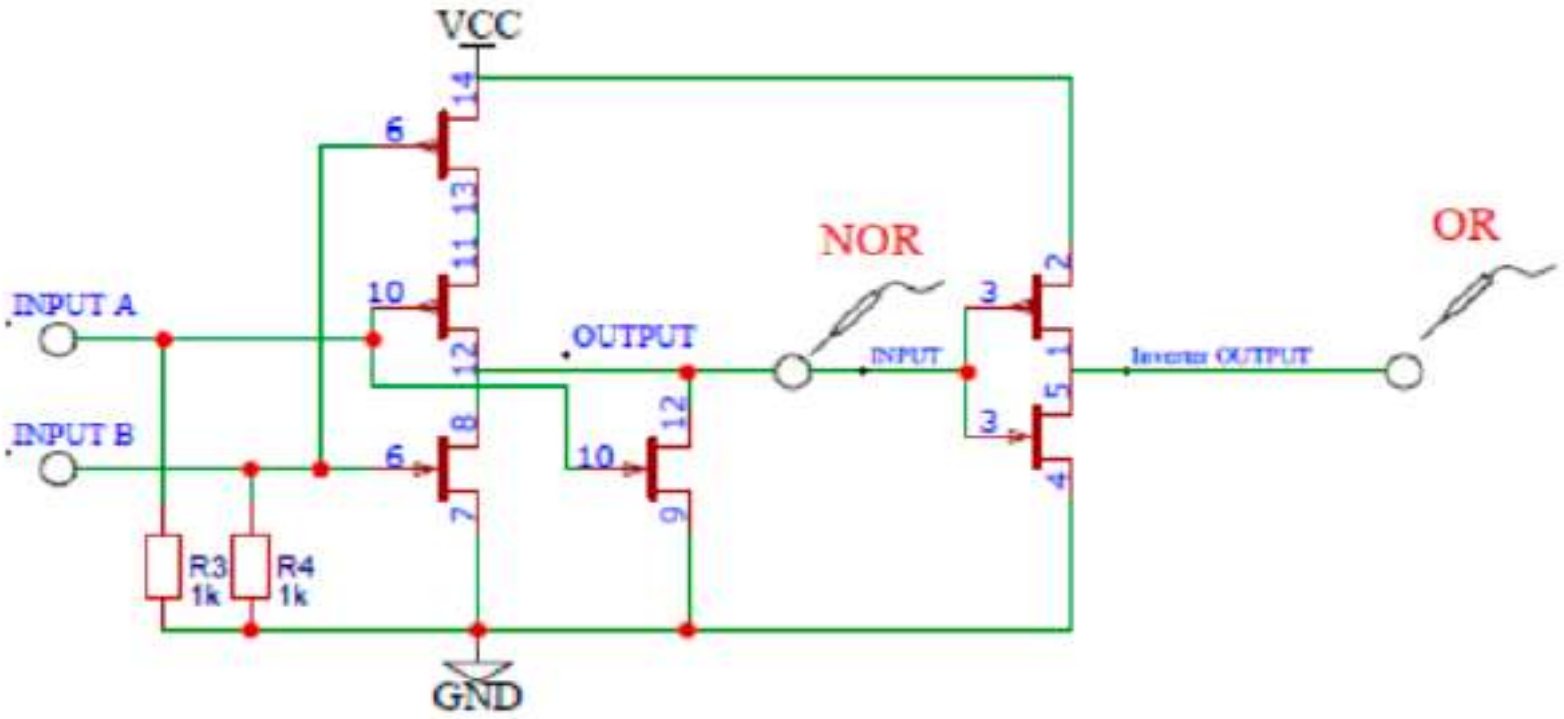


Fig 3: Two inputs gates (NOR, OR) CMOS transistors

Lab practices

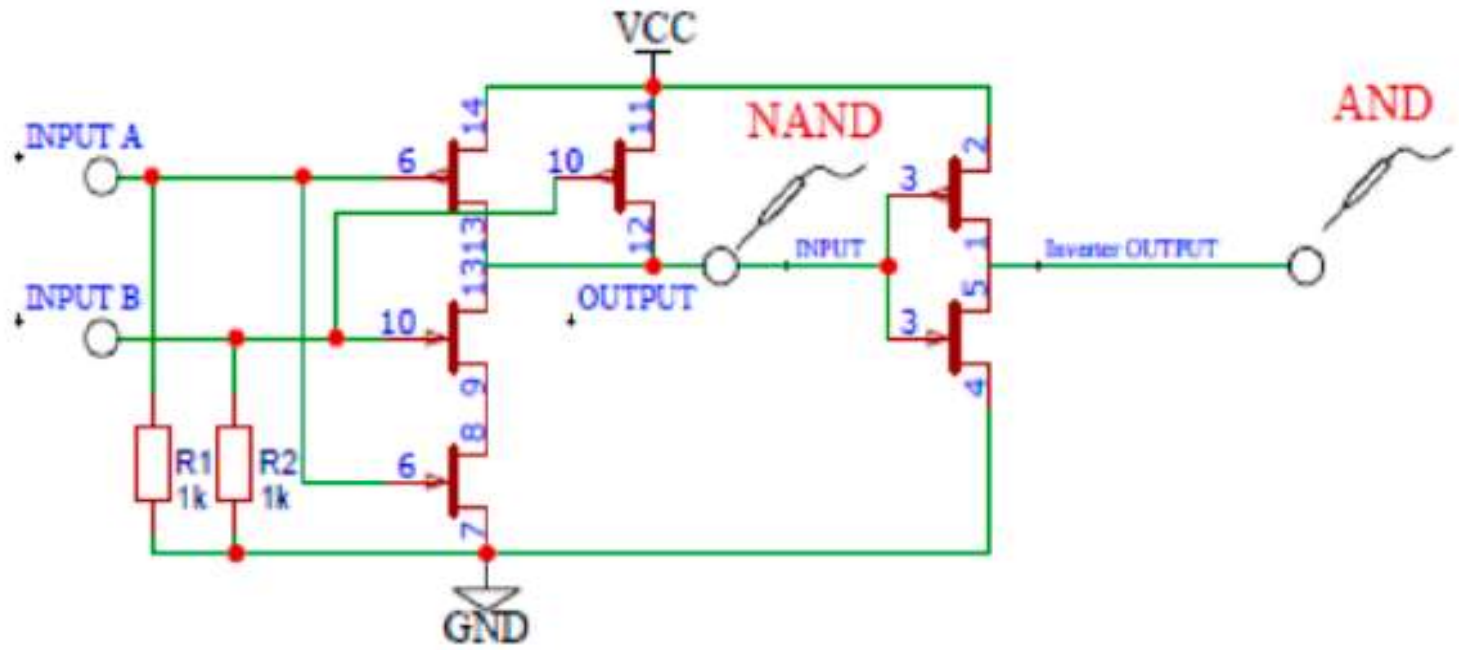


Fig 2: Two inputs gates (NAND, AND) CMOS transistors

Lab practices

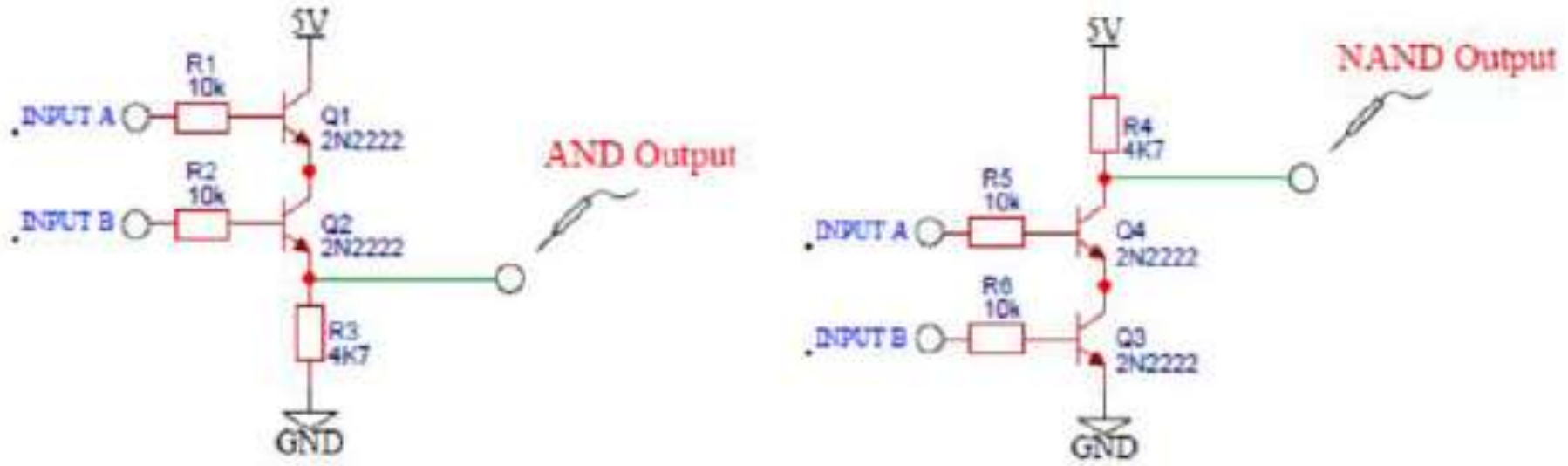


Fig 4: Two inputs gates (AND, NAND) Bipolar transistors

Lab practices

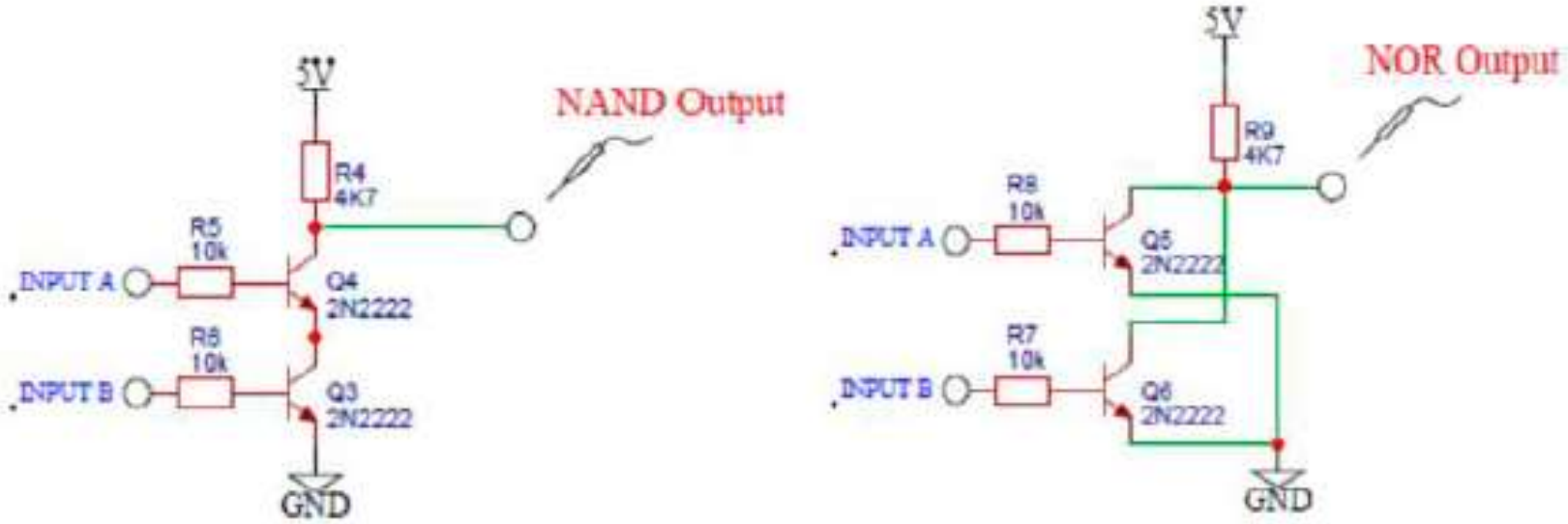


Fig 5: Two inputs gates (OR, NOR) Bipolar transistors

Lab practices

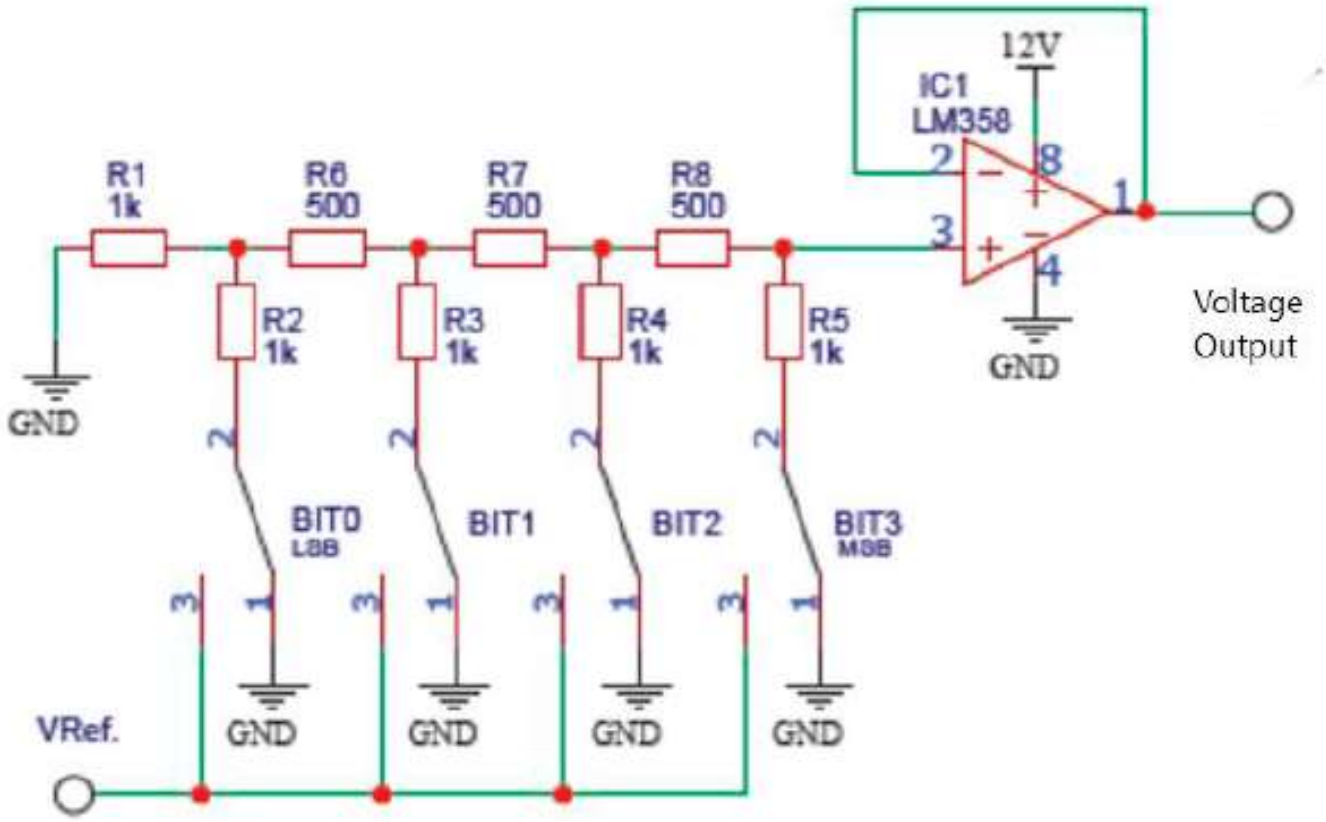


Fig 6: Four bits Digital to Analog R-2R converter

VRef.= 5,11V

BIT3	BIT2	BIT1	BIT0	OUTPUT VOLTAGE MEASURED
0	0	0	0	0
0	0	0	1	0,31
0	0	1	0	0,62
0	0	1	1	0,95
0	1	0	0	1,27
0	1	0	1	1,59
0	1	1	0	1,91
0	1	1	1	2,23
1	0	0	0	2,55
1	0	0	1	2,87
1	0	1	0	3,18
1	0	1	1	3,5
1	1	0	0	3,83
1	1	0	1	4,15
1	1	1	0	4,47
1	1	1	1	4,79

Table 2: Output voltage DAC converter

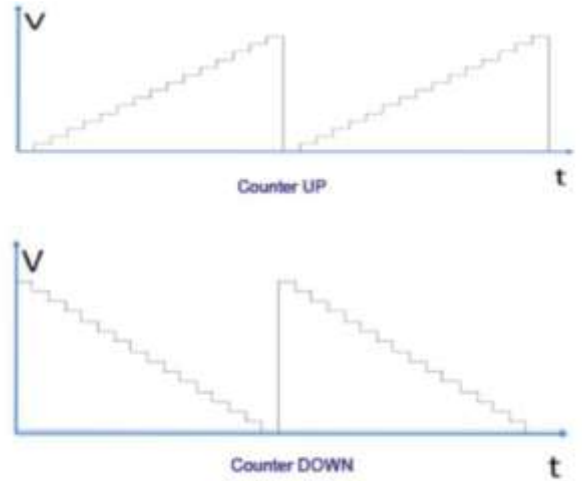


Fig 7: Output voltage screens according SW1 position

Lab practices

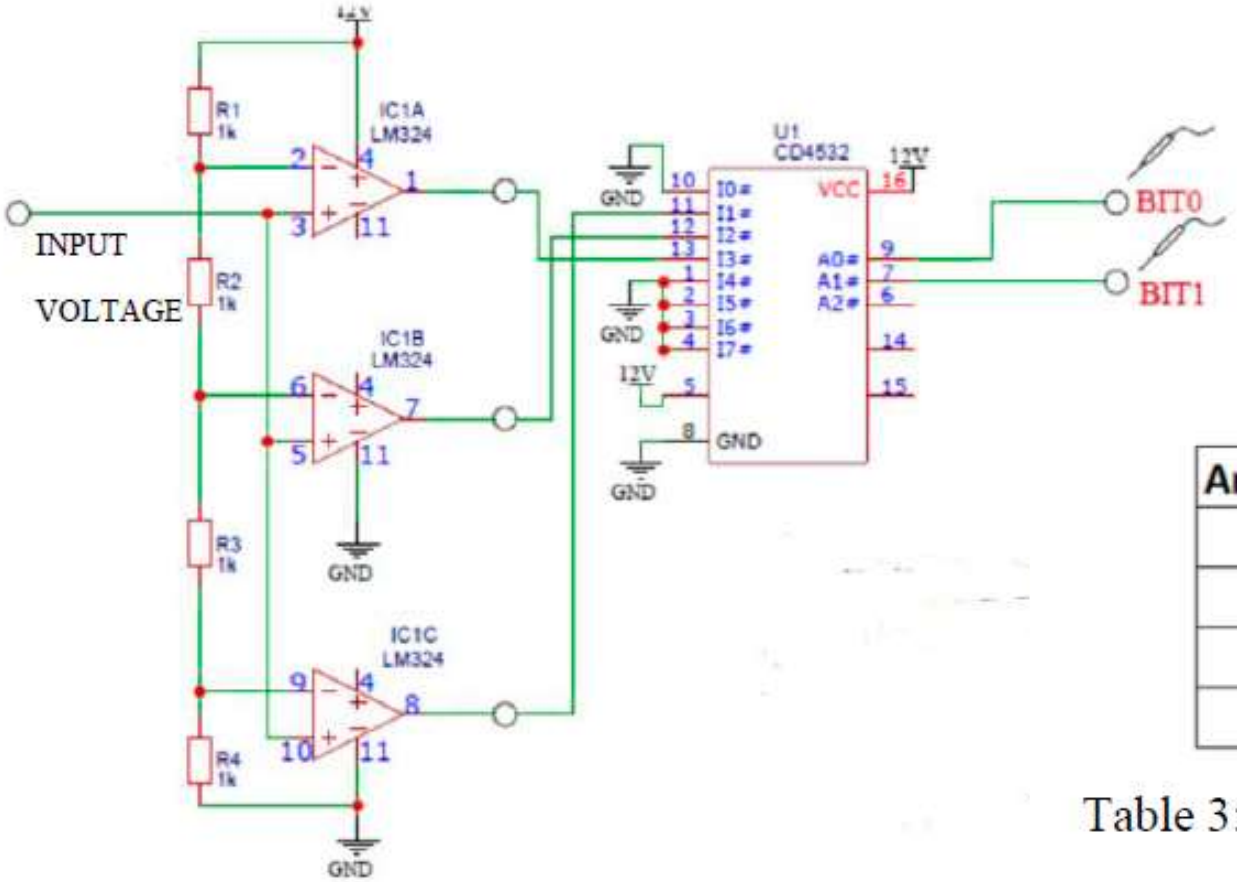


Fig 9: Analog to digital converter

Analog Input Voltage	BIT1	BIT0
0 to 2,9 volts	0	0
3 to 5,8 volts	0	1
5,9 to 8,7 volts	1	0
8,8 to 12 volts	1	1

Table 3: A-D converter output